

List of Figures

2.1	Uplink Transmitter Model	10
2.2	Frame structure for uplink DPDCH/DPCCH	10
2.3	Tapped Delay Line Model	12
2.4	WCDMA Base Station Receiver Model	13
2.5	Block diagram of Multipath searcher	14
2.6	Rake finger components	17
2.7	WMSA Structure	18
2.8	Power delay profiles of three path signals at Doppler speed of 3 km/hr	26
2.9	Performance comparisons of the channel impulse response for path one	27
2.10	Performance comparisons of the channel impulse response for path two	28
2.11	Performance comparisons of the channel impulse response for path three	29
3.1	Conventional SIR Estimator	34
3.2	Adjustable SIR Estimator	37
3.3	Post-Processing Scheme	38
3.4	The Structure of MA Filter	39
3.5	The Structure of EMA Filter	40
3.6	System identification model	44
3.7	Block Diagram of Adaptive Transversal Filter	45
3.8	Detail Structure of the Transversal Filter Component	45
3.9	The Structure of the Adaptive Weight Control Mechanism	46
3.10	Signal flow graph representation of LMS algorithm	48
3.11	The plots of estimated SIR vs the actual SIR using (top) conventional scheme, (middle) adjustable (adaptive) scheme and (bottom) adjustable (adaptive) scheme with MA post-filtering	50

3.12	Signal-to-Interference Ratio vs slot number for Doppler frequency $f_d = 10\text{Hz}$ and tap size $N = 4$	51
3.13	RMSE vs f_d of an Adjustable (adaptive) SIR with and without post-processing stage	52
3.14	(a) Adjustable (adaptive) SIR estimator, (b) LMS Adaptive estimator	52
4.1	Rake receiver components synthesizing by “Xilinx Integrated Software Environment ISE 6.3i”	59
4.2	Rake finger components synthesizing by “Xilinx Integrated Software Environment ISE 6.3i”	60
A.1	Configuration of uplink scrambling sequence generator	76

