Chapter 4

Hardware Implementation

4.1 Background of Downlink Rake Receiver

Since the references or information about hardware implementation for the base station are hardly found. Therefore, in this thesis, we have to adjust some ideas from the downlink hardware implementation.

Bell Labs Algorithm Development and Evaluation (BLADE) presented the prototype for testing WCDMA system by employing the process between the “Digital Signal Processing” (DSP) and “Filed Programmable Gate Array” (FPGA). For FPGA, the circuits are designed to support the data which has high rate and stable (e.g. the circuit of any filters which is employed high bandwidth and high rate for both input and output). In case of DSP, it is used for the case that the information is not stable and the circuit is too complex. The prototype of BLADE is employing 2 chips of the DSP from “Texas Instruments” model 67 and 1 chip of “XCV1000 1000k gate Virtex FPGA” for implementing the downlink of WCDMA system which most of the rake receiver algorithms are implemented on the FPGA. On the other hand, the DSP is used to control the functions of rake finger (Rake finger management) and calculate the coefficient of the filters.

In 2003, Transmission Systems Laboratory Seoul National University presented the prototype which is similar to the BLADE presented above by employing 2 chips of “1 Million Gate Virtex 1000E FPGA” cooperate with 2 chips “TMS320C6202” DSP for implementing the transmitter and the receiver of the mobile in WCDMA system that the receiver circuit has 3 fingers to support 3 path of transmitted signals.

4.2 The Design of Multipath Searcher and Rake receiver circuits on FPGA board

For the hardware implementation, “Modelsim SE 5.6” is used in simulation, the performances are the same as showing in Table 2.3-2.4, while “Xilink Integrated Software Environment ISE 6.3i” is used in case of synthesize the circuit written by using “Very High Speed Integrated Circuits Hardware Description Language (VHDL)” for implementing in FPGA board model “Virtex4 (XC4VLX60)”.

There are 8 main blocks in the Rake receiver, namely, Multipath Searcher, Decimator (downsampling process), OVSF Code Generator, Scrambling Code Generator, Descrambling and Despreading Processes, Channel Estimator, Channel Equalizer, and Maximum Ratio Combining (MRC). In this thesis, we assumed that each rake receiver composed of three main blocks which are one block of multipath searcher, three blocks of rake finger, and one block of MRC. It is noted that decimator, OVSF code generator, scrambling code generator, descrambling and despreading processes, channel estimator, and channel equalizer are located in rake finger. Resource consumption of each block are shown in Table 4.2.

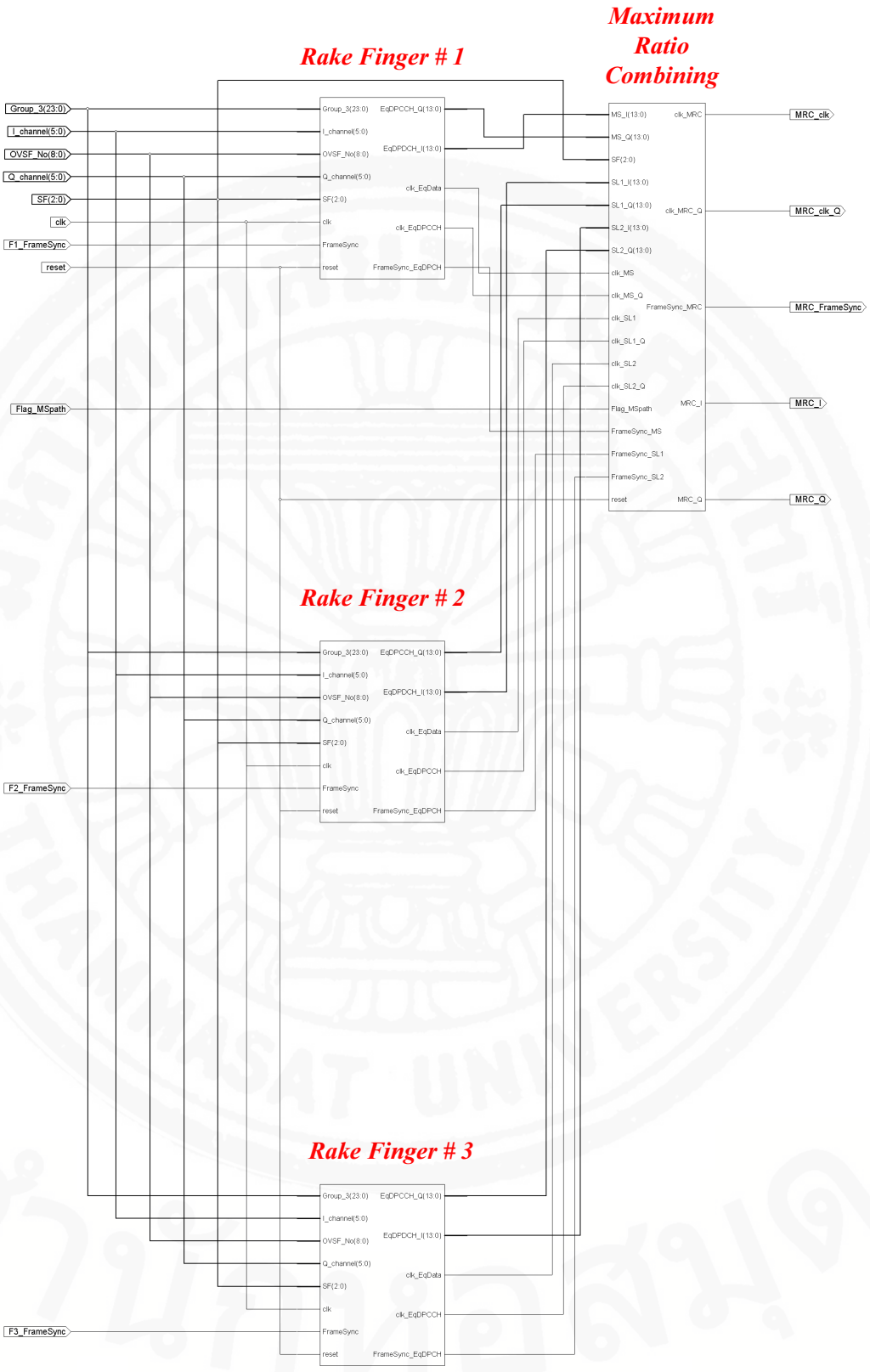

Figure 4.1 Rake receiver components synthesizing by “Xilink Integrated Software Environment ISE 6.3i”

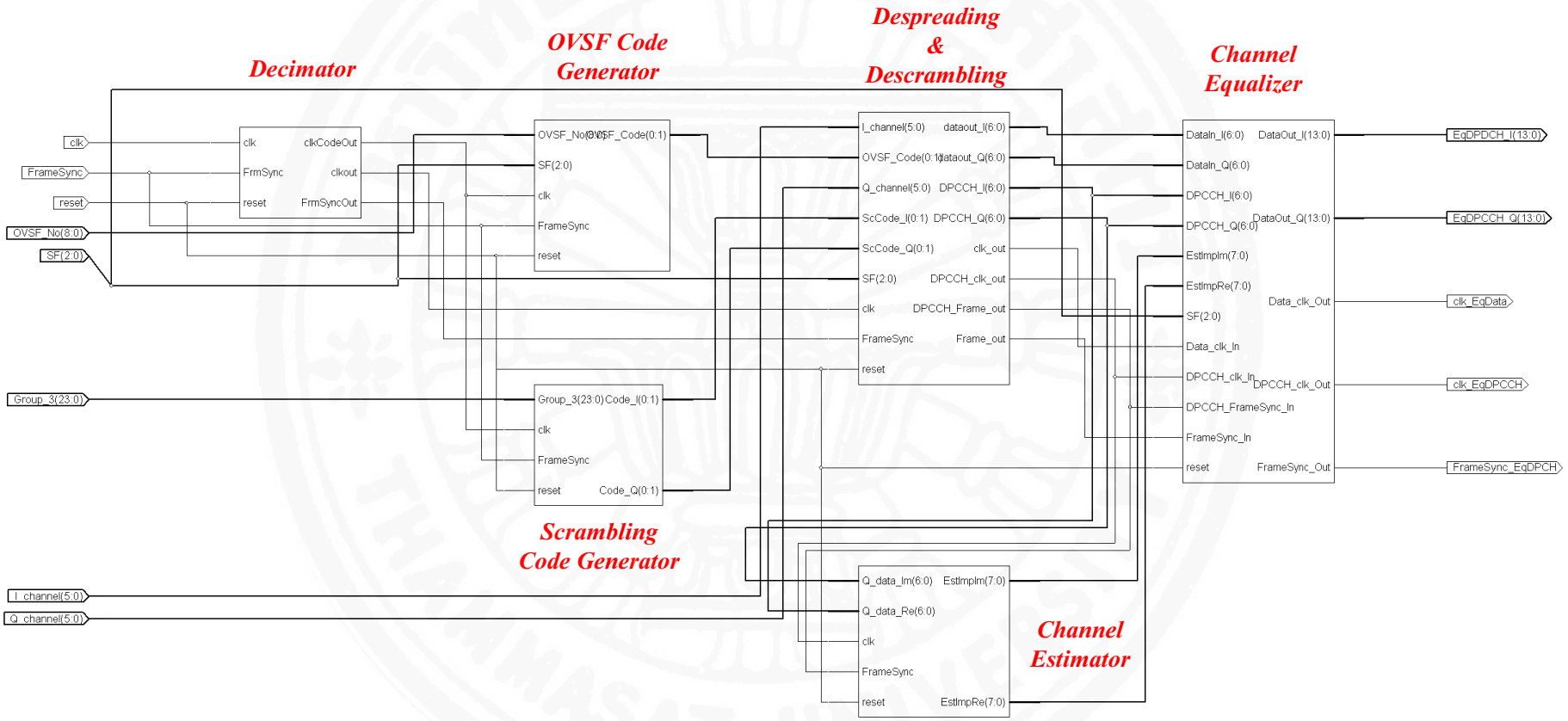

Figure 4.2 Rake finger components synthesizing by “Xilink Integrated Software Environment ISE 6.3i”

Figure 4.1 and Figure 4.2 show the components of rake receiver and rake finger respectively, by using software named “Xilink Integrated Software Environment ISE 6.3i” to synthesize.

Table 4.1 Input and Output signals of Base Station Circuit

Input signals received from Baseband	
$reset$	Reset signal
$FrameSync1$	Frame synchronization signal
clk	Clock signal sent from baseband
$I-channel<5:0>$	In-phase digital signal (6 bits)
$Q-channel<5:0>$	Quadrature digital signal (6 bits)
$SerialFrame-Rx$	Serial interface of frame setting
$SerialData-Rx$	Serial interface of data setting
$SerialClk-Rx$	Serial interface of clock setting
Output signals sent to Baseband	
$MRCFrameSync$	Frame synchronization signal from MRC
$DPDCH$	Decoded in-phase signal
$Clk-DPDCH$	Clock signal of an in-phase signal
$DPCCH$	Decoded quadrature signal
$Clk-DPCCH$	Clock signal of a quadrature signal

Table 4.1 shows the input and output signals for the base station designed by using VHDL codes.

4.3 Resources usage

This section shows the table for resources consumption of FPGA board model “Virtex4 (XC4VLX60)” (Table 4.2) which is synthesized by using “Xilink Integrated Software Environment ISE 6.3i”.

Table 4.2 Resource Consumption

Component	Percentage (%)						Maximum Frequency (MHz)
	Slices	Flip Flops	Input LUTs	Bonded IOBs	FIFO16/ RAMB16s	GCLKs	
Multipath Searcher	21	5	19	4	40	6	60.108
Decimator	1	1	1	1	N/A	3	205.387
OVSF Code Generator	1	1	1	3	N/A	3	125.578
Scrambling Code Generator	1	1	1	6	N/A	3	377.430
Descrambling and Despreading Processes	1	1	1	12	N/A	3	98.127
Channel Estimator	3	1	3	7	N/A	3	91.245
Channel Equalizer	1	1	1	18	3	6	54.380
Rake Finger	6	2	6	18	3	15	54.380
Maximum Ratio Combining	6	3	2	22	N/A	9	89.536
Rake Receiver	45	16	39	13	40	50	54.380