Appendix F

The Design of Base Station Receiver by Using VHDL Code

Program Description

Input:

- Reset signal.
- Frame synchronization signal.
- Clock signal sent from baseband.
- In-phase digital signal (6 bits).
- Quadrature digital signal (6 bits).
- Serial interface of frame setting.
- Serial interface of data setting.
- Serial interface of clock setting.

Output:

- Frame synchronization signal from MRC.
- Decoded in-phase signal.
- Clock signal of an in-phase signal.
- Decoded quadrature signal.
- Clock signal of a quadrature signal.

```
LIBRARY ieee; USE ieee.std_logic_1164.all; USE
ieee.std_logic_arith.all; USE ieee.std_logic_signed.all;

ENTITY ULBase_For2User IS
    Port (  reset : IN std_logic;                   -- reset signal from G3 or reset switch
        FrameSync1_user1 : IN std_logic;            -- FrameSync for Finger1 of User1 (from Wantawat)
        FrameSync1_user2 : IN std_logic;            -- FrameSync for finger1 of User2 (from Wantawat)
        clk : IN std_logic;                 -- clk 15.36 MHz
        I_channel : IN std_logic_vector(5 downto 0);        -- Input I_channel
        Q_channel : IN std_logic_vector(5 downto 0);        -- Input Q_channel
        SerialFrame_Rx : IN std_logic;              -- Serial Interface of Parameter setting from G3
        SerialData_Rx  : IN std_logic;
        SerialClk_Rx   : IN std_logic;

        User1_MRCFrameSync : OUT std_logic;         -- User1's output to G3
        User1_DPDCH : OUT std_logic;
        User1_Clk_DPDCH : OUT std_logic;
        User1_DPCCH : OUT std_logic;
        User1_Clk_DPCCH : OUT std_logic;

        User2_MRCFrameSync : OUT std_logic;         -- User2's output to G3
        User2_DPDCH : OUT std_logic;
        User2_Clk_DPDCH : OUT std_logic;
        User2_DPCCH : OUT std_logic;
        User2_Clk_DPCCH : OUT std_logic
        );
END ULBase_For2User;

ARCHITECTURE behavior OF ULBase_For2User IS
    COMPONENT SerialRx_Prm
    Port (
            SerialFrame_Rx : in std_logic;
            SerialData_Rx  : in std_logic;
            SerialClk_Rx   : in std_logic;

        User1_ScCodeNumber : out std_logic_vector(23 downto 0);     -- User1's Scrambling Code Number
        User2_ScCodeNumber : out std_logic_vector(23 downto 0);     -- User2's Scrambling Code Number
        User1_SF : out std_logic_vector(2 downto 0);            -- User1's DPDCH Spreading Factor
        User2_SF : out std_logic_vector(2 downto 0);            -- User2's DPDCH Spreading Factor
        User1_OVSF_No : out std_logic_vector(8 downto 0);       -- User1's DPDCH Spreading Code number
        User2_OVSF_No : out std_logic_vector(8 downto 0)        -- User2's DPDCH Spreading Code number
    );
    END COMPONENT;

    COMPONENT Block_ULmultipathsearcher
    PORT (  reset : IN std_logic;
        FrameSync : IN std_logic;               -- Finger1's FrameSync (from Wantawath)
        clk : IN std_logic;                 -- clk 15.36 MHz
        I_channel : IN std_logic_vector(5 downto 0);        -- Input I_channel
        Q_channel : IN std_logic_vector(5 downto 0);        -- Input Q_channel
        ScCode_number : IN std_logic_vector(23 downto 0);   -- Scrambling Code Number
        FrameSync_Finger2 : OUT std_logic;          -- Finger2's FrameSync (output)
        FrameSync_Finger3 : OUT std_logic           -- Finger3's FrameSync (output)
        );
    END COMPONENT;

    COMPONENT Rake_Receiver
    PORT (  reset : IN std_logic;
        Flag_MSpath : IN std_logic;
        F1_FrameSync : IN std_logic;
        F2_FrameSync : IN std_logic;
        F3_FrameSync : IN std_logic;
        clk : IN std_logic;
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        I_channel : IN std_logic_vector(5 downto 0);
        Q_channel : IN std_logic_vector(5 downto 0);
        Group_3 : IN std_logic_vector(23 downto 0);
        SF : IN std_logic_vector(2 downto 0);
        OVSF_No : IN std_logic_vector(8 downto 0);

        MRC_FrameSync : OUT std_logic;
        MRC_clk : OUT std_logic;
        MRC_I : OUT std_logic;
        MRC_clk_Q : OUT std_logic;
        MRC_Q : OUT std_logic
        );
    END COMPONENT;

    ------------------------------------------------------------------------------------------
    ----- Global signal ------------------------------------------------------------------
    ------------------------------------------------------------------------------------------

    -- (Output from Wantawat's Uplink Frame Synchronization circuit)
--  signal FrameSync1_user1 : std_logic := '0'; --  signal
FrameSync1_user2 : std_logic := '0';

    -- Parameter from G3 via Serial Interface --
    signal User1_ScCodeNumber : std_logic_vector(23 downto 0):= (others=>'0');
    signal User2_ScCodeNumber : std_logic_vector(23 downto 0):= (others=>'0');
    signal User1_SF : std_logic_vector(2 downto 0):= "000";
    signal User2_SF : std_logic_vector(2 downto 0):= "000";
    signal User1_OVSF_No : std_logic_vector(8 downto 0):= (others=>'0');
    signal User2_OVSF_No : std_logic_vector(8 downto 0):= (others=>'0');

    -- (Inputs which are outputs of UL_Multipathsearcher)---
    signal Flag_MSpath : std_logic:= '0';
    signal User1_FrameSync_Finger2 : std_logic := '0';
    signal User1_FrameSync_Finger3 : std_logic := '0';
    signal User2_FrameSync_Finger2 : std_logic := '0';
    signal User2_FrameSync_Finger3 : std_logic := '0';
    ------------------------------------------------------------------------------------------

    FOR Serial_Interface : SerialRx_Prm USE ENTITY work.SerialRx_Prm(Behavior);
    FOR User1_ULPathSearch :
    Block_ULmultipathsearcher USE ENTITY work.Block_ULmultipathsearcher(behavior);
    FOR User2_ULPathSearch :
    Block_ULmultipathsearcher USE ENTITY work.Block_ULmultipathsearcher(behavior);
    FOR User1_ULRakeReceiver : Rake_Receiver USE ENTITY work.Rake_Receiver(behavior);
    FOR User2_ULRakeReceiver : Rake_Receiver USE ENTITY work.Rake_Receiver(behavior);

BEGIN
    Serial_Interface : SerialRx_Prm PORT MAP
                ( SerialFrame_Rx,
                  SerialData_Rx,
                  SerialClk_Rx,
                  User1_ScCodeNumber,
                  User2_ScCodeNumber,
                  User1_SF,
                  User2_SF,
                  User1_OVSF_No,
                  User2_OVSF_No
                  );

    User1_ULPathSearch : Block_ULmultipathsearcher PORT MAP
                ( reset,
                  FrameSync1_user1,
                  clk,
                  I_channel,
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                Q_channel,
                User1_ScCodeNumber,
                User1_FrameSync_Finger2,
                User1_FrameSync_Finger3
                );

    User2_ULPathSearch : Block_ULmultipathsearcher PORT MAP
                ( reset,
                FrameSync1_user2,
                clk,
                I_channel,
                Q_channel,
                User2_ScCodeNumber,
                User2_FrameSync_Finger2,
                User2_FrameSync_Finger3
                );

    User1_ULRakeReceiver : Rake_Receiver PORT MAP
                ( reset,
                Flag_MSpath,
                FrameSync1_user1,
                User1_FrameSync_Finger2,
                User1_FrameSync_Finger3,
                clk,
                I_channel,
                Q_channel,
                User1_ScCodeNumber,
                User1_SF,
                User1_OVSF_No,
                User1_MRCFrameSync,
                User1_Clk_DPDCH,
                User1_DPDCH,
                User1_Clk_DPCCH,
                User1_DPCCH
                );

    User2_ULRakeReceiver : Rake_Receiver PORT MAP
                ( reset,
                Flag_MSpath,
                FrameSync1_user2,
                User2_FrameSync_Finger2,
                User2_FrameSync_Finger3,
                clk,
                I_channel,
                Q_channel,
                User2_ScCodeNumber,
                User2_SF,
                User2_OVSF_No,
                User2_MRCFrameSync,
                User2_Clk_DPDCH,
                User2_DPDCH,
                User2_Clk_DPCCH,
                User2_DPCCH
                );
END behavior;
```