Chapter 7

Conclusions

7.1 Summary

Coherent schemes for PN code timing synchronization in DS/SS systems were studied in this thesis. The motivation and scope were addressed in Chapter 1. Chapter 2 was devoted to review the literature on both PN code acquisition and PN code tracking circuit.

In Chapter 3, two modified coherent extended range DLLs, called PelDLL and PerDLL, were proposed. Both were designed to cover code phase difference of up to four chips. The proposed schemes applied branch selection algorithms to select the branch for code phase tracking. The PelDLL consisted of three branches, each correlated the received signal with a local signal of different code phase. The code phase corresponding to the branch possessing the maximum absolute correlation output was selected as the initial code phase for the tracking circuit. The loop characteristic of each branch was similar to the conventional early-late DLL. The structure of PerDLL is similar to PelDLL, except that the branch selection algorithm was based on the minimum absolute value and the loop characteristic of each branch behaved like the conventional extended DLL. Since the branch selection was used, the tracking jitter and mean time to lose lock were the same as those in conventional coherent early-late DLL. The performances of the proposed schemes were evaluated using the probability of correct branch selection and compared to a previous branch-selection DLL, called SelDLL. Results showed that the proposed schemes offered higher probability of correct branch selection.

A coherent PN code acquisition with sectional code phase estimator was proposed in Chapter 4. The proposed scheme consisted of a sectional code phase estimator and an alignment detector. The code phase uncertainty region is divided into 2^M sections, where M is the number of correlator branches in the code phase estimator. The code phase estimator used a set of auxiliary signals to choose one of the sections as an estimate of the uncertainty section that the correct code phase is most likely located. The estimated section was supplied to the alignment detector, where the correct code phase was searched. The code phase estimator periodically provided a new estimated section until the alignment detector found the correct code phase. The performance of the sectional code phase estimator was evaluated using the probability of correct estimate. In our design, the correct code phase can also be detected if the estimated section is a detectable incorrect estimate, which is a neighboring section of the correct section. The estimator uses not only the new correlation results, but also the results used in previous estimate, i.e., all the available results. The probabilities of the correct estimate as well as a detectable incorrect estimate were derived in this chapter. Furthermore, the probabilities of non-detectable incorrect estimate were also provided.

The acquisition time analysis of the proposed coherent acquisition scheme described in Chapter 4 was presented in Chapter 5. The analysis applied the signal flow graph technique. The signal flow graph of the proposed acquisition scheme involved many probabilities and transfer functions. These probabilities were already given in Chapter 4.

The transfer functions were derived Chapter 5. The pmf and mean of the acquisition time were obtained straightforwardly from the signal flow graph of the proposed system.

Performance evaluations of the proposed acquisition scheme were shown in Chapter 6. Both unconditional and conditional probabilities of the phase estimator given in Chapter 4 were investigated in detail. The effective performance of the proposed acquisition system was appraised using the mean of the acquisition time (MAT) and variance of the acquisition time (VAT). The analytical MAT given in Chapter 5 was compared with the simulation result. Both agree well. The improvement of both MAT and VAT over those of the single dwell serial search scheme was shown. Several folds and tens folds of the MAT ratio and VAT ratio were obtained, depending on the choices of the parameter.

7.2 Further Topics for Future Research

Several extended topics can be studied further. These can be mentioned as follows.

(i) Modify the proposed schemes to the case with noncoherent carrier demodulation.

(ii) Investigate the performance of the proposed schemes in the presence of data modulation, carrier Doppler, and code Doppler. And therefore, design new schemes to overcome these problems.

(iii) Investigate the performance of the proposed scheme in a multipath and fading channel, and multiple access environment. Then, design new schemes to overcome these problems.

(iv) Investigate the performance of the proposed scheme when using other kinds of PN codes, such as Gold code. Then, modified the scheme for other specific PN code.

(v) Combine other techniques, such as antenna diversity, rake structure, etc. to the proposed scheme. Evaluate the performance and design a suitable scheme.

(vi) Design a joint receiver structure that performs the code tracking, carrier tracking, and data detection at the same time.

(vii) Design a hybrid PelDLL/PerDLL code tracking system that combines the advantages of both PelDLL and PerDLL.

(viii) Modified the proposed acquisition scheme presented in Chapter 4 to use other kinds of detector, such as the multiple dwell and sequential detectors, etc.